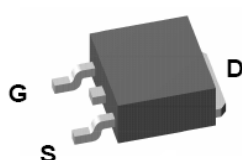


# P6010DDG

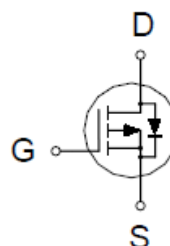
## P-Channel Logic Level Enhancement Mode MOSFET

### PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	$I_D$
-100V	60mΩ @ $V_{GS} = -10V$	-20A



TO-252



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		$V_{DS}$	-100	V
Gate-Source Voltage		$V_{GS}$	±20	
Continuous Drain Current	$T_C = 25\text{ }^{\circ}\text{C}$	$I_D$	-20	A
	$T_C = 100\text{ }^{\circ}\text{C}$		-12	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	-60	
Avalanche Current		$I_{AS}$	-54	
Avalanche Energy	$L = 0.1\text{mH}$	$E_{AS}$	149	mJ
Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	$P_D$	50	W
	$T_C = 100\text{ }^{\circ}\text{C}$		20	
Operating Junction & Storage Temperature Range		$T_J, T_{STG}$	-55 to 150	$^{\circ}\text{C}$

### THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		2.5	$^{\circ}\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		75	

<sup>1</sup>Pulse width limited by maximum junction temperature.

# P6010DDG

## P-Channel Logic Level Enhancement Mode MOSFET

### ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C, Unless Otherwise Noted)

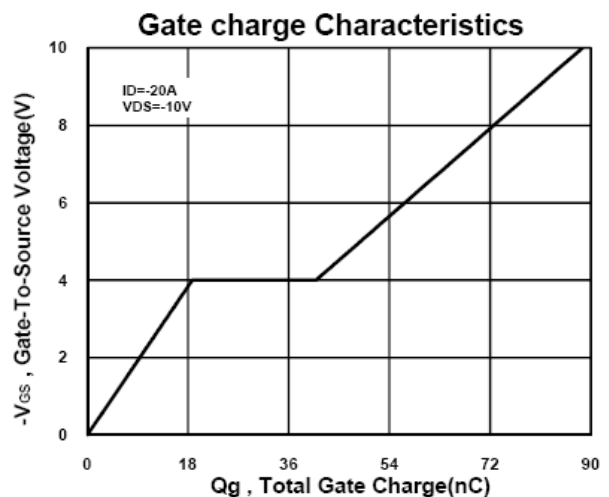
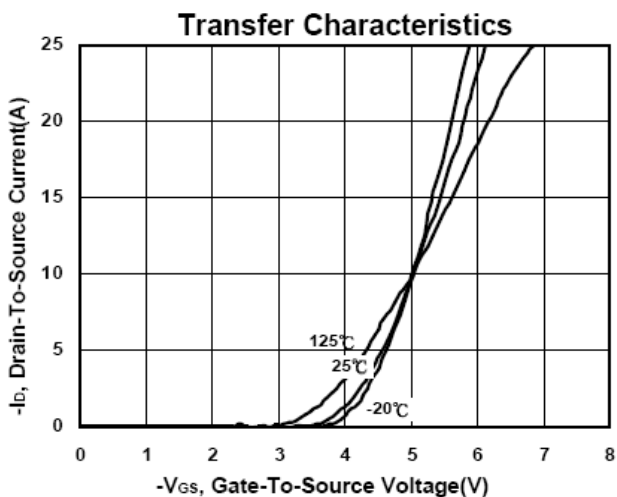
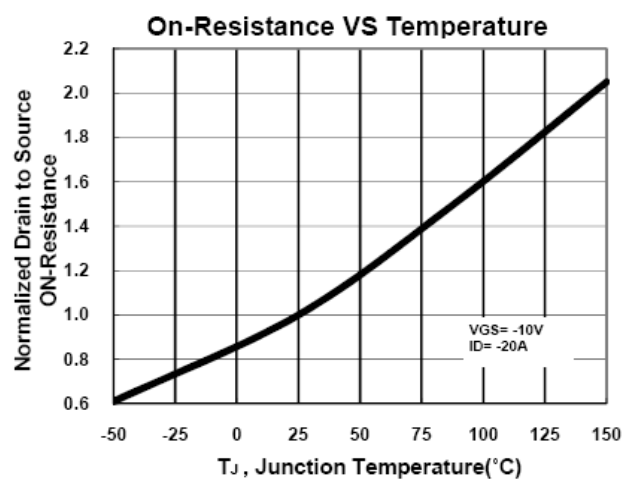
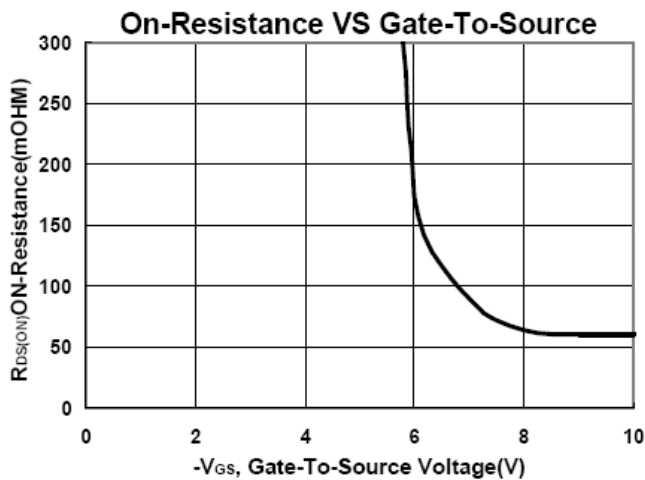
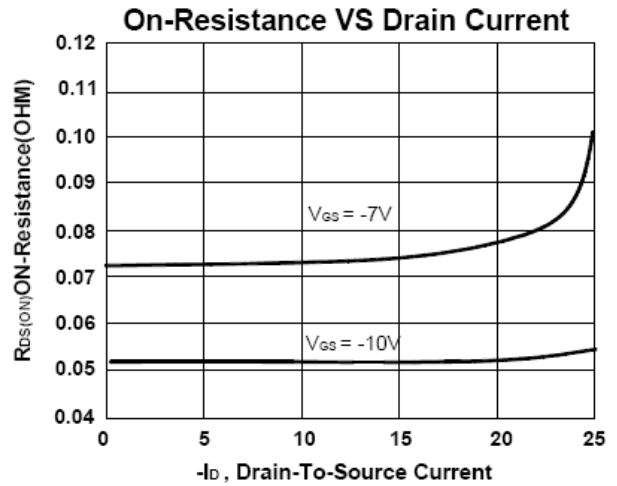
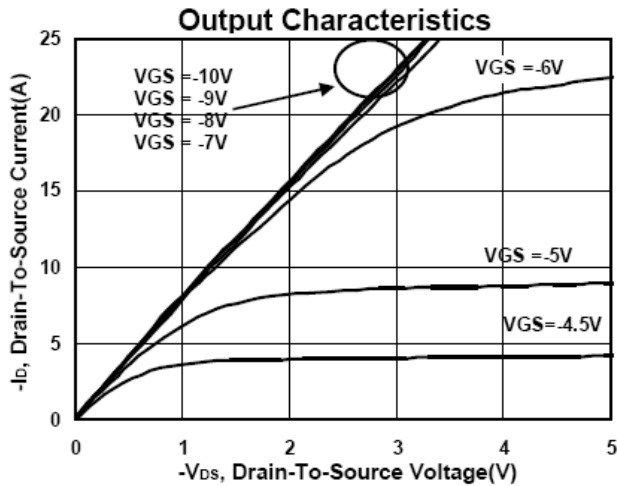
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.5	-2.7	-4	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$			$\pm 250$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -80V, V_{GS} = 0V$			-1	$\mu A$
		$V_{DS} = -80V, V_{GS} = 0V, T_J = 125^\circ C$			-10	
On-State Drain Current <sup>1</sup>	$I_{D(ON)}$	$V_{DS} = -5V, V_{GS} = -10V$	-60			A
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(ON)}$	$V_{GS} = -7V, I_D = -18A$		53	72	mΩ
		$V_{GS} = -10V, I_D = -20A$		51	60	
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = -5V, I_D = -20A$		35		S
DYNAMIC						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = -25V, f = 1MHz$		4960		pF
Output Capacitance	$C_{oss}$			224		
Reverse Transfer Capacitance	$C_{rss}$			167		
Gate Resistance	$R_g$	$V_{GS} = 0V, V_{DS} = 0V, f = 1MHz$		4.6		Ω
Total Gate Charge <sup>2</sup>	$Q_g$	$V_{DS} = 0.5V_{(BR)DSS}, V_{GS} = -10V, I_D = -20A$		90		nC
Gate-Source Charge <sup>2</sup>	$Q_{gs}$			19		
Gate-Drain Charge <sup>2</sup>	$Q_{gd}$			24		
Turn-On Delay Time <sup>2</sup>	$t_{d(on)}$	$V_{DS} = -20V, I_D \cong -1A, V_{GS} = -10V, R_{GS} = 6\Omega$		20		nS
Rise Time <sup>2</sup>	$t_r$			25		
Turn-Off Delay Time <sup>2</sup>	$t_{d(off)}$			120		
Fall Time <sup>2</sup>	$t_f$			125		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ( $T_J = 25^\circ C$ )						
Continuous Current	$I_S$				-20	A
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = -20A, V_{GS} = 0V$			-1.3	V
Reverse Recovery Time	$t_{rr}$	$I_F = -20A, dI_F/dt = 100A / \mu S$		84.3		nS
Reverse Recovery Charge	$Q_{rr}$			256		nC

<sup>1</sup>Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

<sup>2</sup>Independent of operating temperature.

## P6010DDG

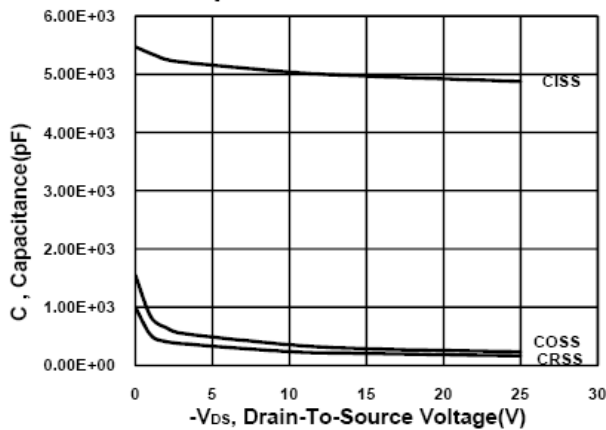
### P-Channel Logic Level Enhancement Mode MOSFET



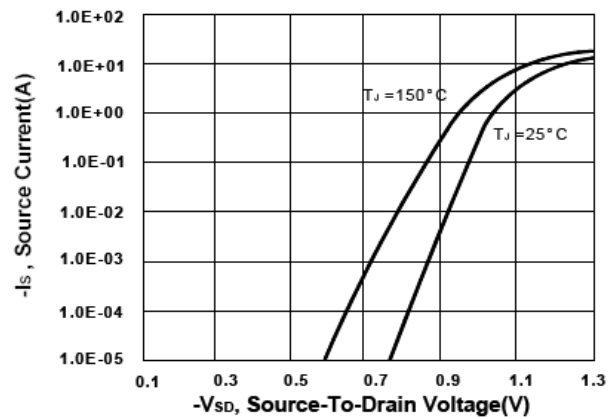
# P6010DDG

## P-Channel Logic Level Enhancement Mode MOSFET

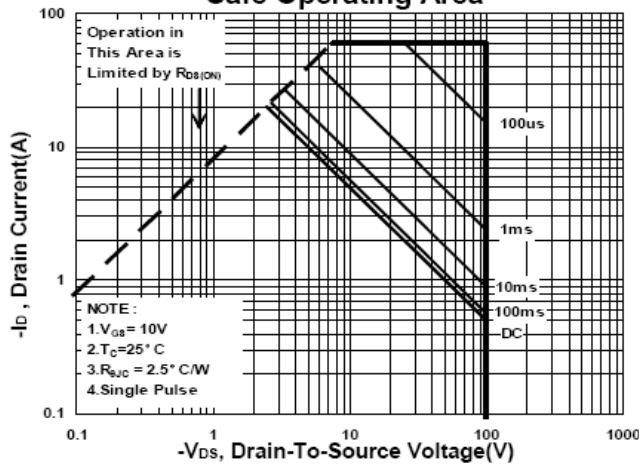
**Capacitance Characteristic**



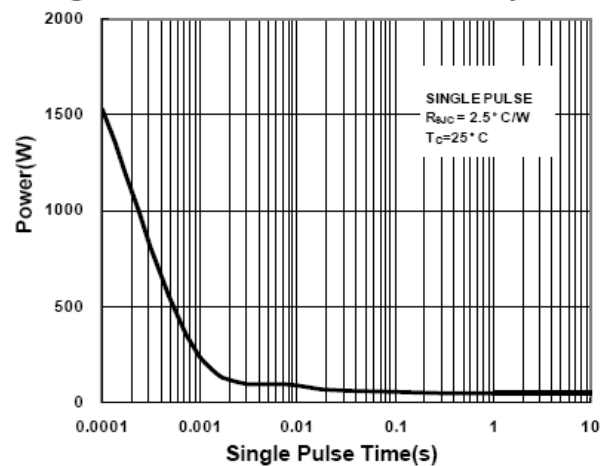
**Body Diode Forward Voltage VS Source current**



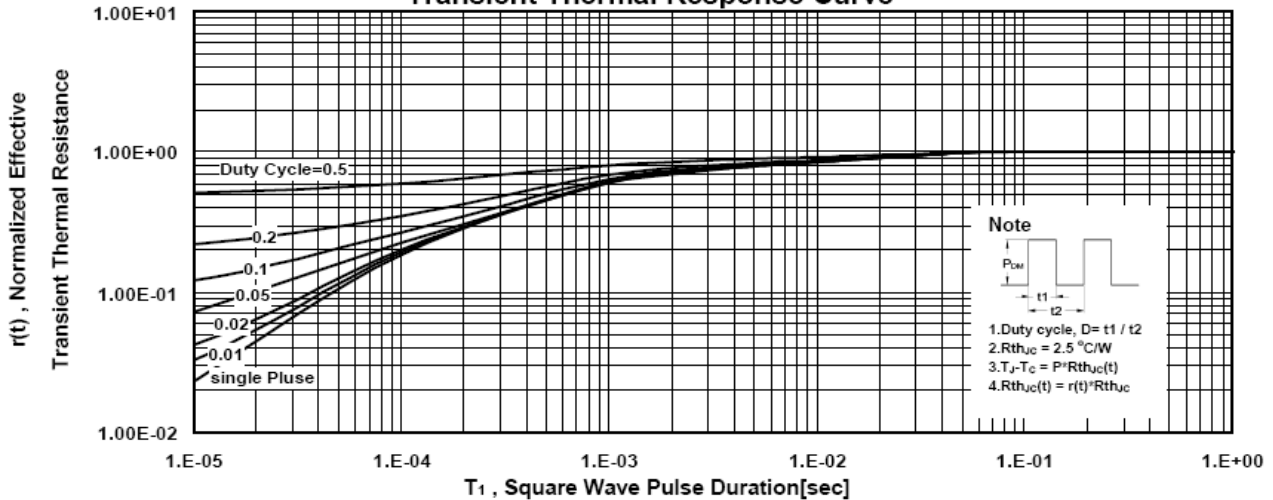
**Safe Operating Area**



**Single Pulse Maximum Power Dissipation**



**Transient Thermal Response Curve**



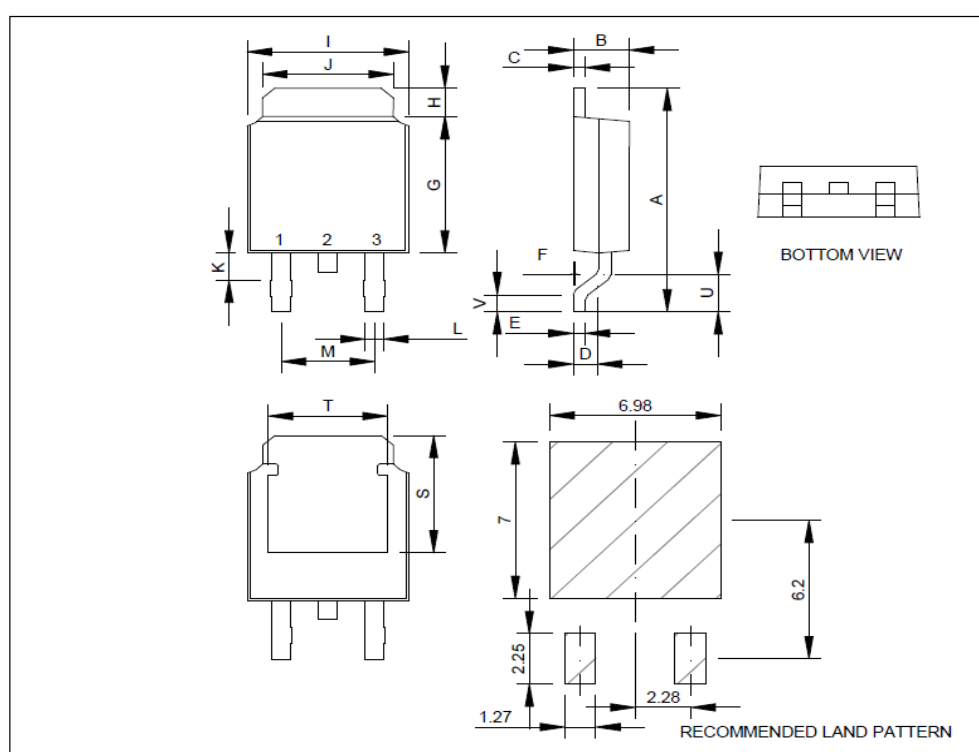
# P6010DDG

## P-Channel Logic Level Enhancement Mode MOSFET

### Package Dimension

### TO-252 (DPAK) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	8.9	10	10.41	J	4.8		5.64
B	2.1	2.2	2.4	K	0.15		1.1
C	0.4	0.5	0.61	L	0.4	0.76	0.89
D	0.82	1.2	1.5	M	4.2	4.58	5
E	0.4	0.5	0.61	S	4.9	5.1	5.3
F	0		0.2	T	4.6	4.75	5.44
G	5.3	6.1	6.3	U	1.4		1.78
H	0.9		1.7	V	0.55	1.25	1.7
I	6.3	6.5	6.8				



\*因为各家封装模具不同而外观略有所差异，不影响电性及Layout。